CLAIMS

1. A digital video signal processor having an input adapted to receive a digital video signal having first timing signal references at fixed first locations within the line and picture structure; a timing reference stripper for removing said first timing signal references from the digital video signal and a timing reference processor for inserting second timing signal references into the video signal at locations other than said first locations.

2. A processor according to Claim 1, wherein said second timing signal references are substantially fewer in number than said first timing signal references.

3. A processor according to Claim 1, wherein said first timing signal references comprise start of line and end of line references and said second timing signal references are inserted substantially once per picture.

4. A processor according to any one of the preceding claims, wherein substantially every second timing signal reference includes information concerning the number of lines per picture within the digital video signal.

5. A processor according to any one of the preceding claims, wherein substantially every second timing signal reference includes information concerning the length of each line within the digital video signal.

6. A processor according to any one of the preceding claims, wherein substantially every second timing signal reference includes information concerning the aspect ratio of the picture.

7. A processor according to any one of the preceding claims, wherein substantially all the second timing signal references are identical.

8. A digital video signal processing system comprising an output component adapted to receive a digital video signal having first timing signal references at fixed first locations within the line and picture structure, to remove said first timing signal references and insert second timing signal references at locations other than said first locations; and an input component adapted to receive a digital video signal having said second timing signal references, to remove said second timing signal references and to derive from said second timing signal references appropriate timing references for use in further processing of the digital video signal.

9. A digital video interface substantially in accordance with ITU/R Recommendation 656, or other digital video standard, characterised in that timing reference signals are transmitted less than twice per line in order to inhibit unauthorised use of the video information.

10. A digital video interface as described in Claim 9 where no timing reference signal corresponds to the start or finish of a digital active line.

11. A digital video interface in accordance with either Claim 9 or Claim 10 in which the timing reference signals are identical.

12. A digital video interface in accordance with either Claim 9 or Claim 10 in there is no explicit F, V and H information in the timing reference signals.

13. A digital video interface in accordance with any one of Claims 9 to 12, in which aspect ratio information is carried in the timing reference signals.

14. A digital video interface in accordance with any one of Claims 9 to 13 in which line standard information is carried in the timing reference signals.

15. A digital video interface in accordance with any one of Claims 9 to 14 in which the timing reference signals include data identifying a method of scrambling.

16. A digital video interface in accordance with any one of Claims 9 to 15 in which the order of significance of the bits is rearranged.

17. A digital video interface in accordance with Claim 16 in which the order of significance of the bits is rearranged according to a predictable pattern.

18. A digital video interface in which data words are scrambled by an process which substitutes alternative data words for input data words in a manner known only to authorised recipients of the video, characterised in that specific words are prevented from being transmitted by re-submitting them to the scrambling process repeatedly until a valid word is obtained.

19. A digital video interface in which data words are scrambled by a process which substitutes alternative data words for input data words in a manner known only to authorised recipients of the video, characterised in that specific words are prevented from being transmitted by replacing them with unscrambled words.

20. A digital video interface in accordance with Claim 19 in which invalid unscrambled words are replaced by the corresponding inputs words to the unscrambling process.

21. A digital video signal processor having an input adapted to receive a video signal and a timing reference processor for inserting timing references into the video signal, the timing references being substantially identical and appearing substantially once per picture.

22. An scrambled video signal in accordance with any of the preceding claims.